A *K*-Band GaAs FET Amplifier with 8.2-W Output Power

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Abstract—**An 8.2-W GaAs FET amplifier with 38.6 ± 0.5-dB gain over a 17.7–19.1-GHz frequency band has been developed. This amplifier combines the outputs of eight multistage amplifier modules utilizing a radial combiner. This state-of-the-art power level has been achieved with AM/PM of less than 2°/dB. The third-order intermodulation products at 1-dB gain compression were 20 dBc, and variation in group delay over the frequency band was less than ± 0.25 ns. Tests show that the amplifier is unconditionally stable and follows the graceful degradation principle.**

I. Introduction

STUDIES OF THE GROWTH in communications traffic indicate that the frequency spectrum allocated to fixed-service satellites at *C*- and *Ku*-bands will reach saturation by the early 1990's. *K*-band, with uplink frequencies at 27.5–30.0 GHz and downlink frequencies at 17.7–20.2 GHz, is the next higher frequency band allocated for this purpose [1].

System studies have identified the use of multibeam antenna systems as a major factor in achieving minimum cost and efficient use of frequency and orbital resources. Such multibeam systems, however, require reliable, efficient, lightweight, solid-state transmitters.

With the recent advances in GaAs power FET technology [2] at higher frequencies and with the use of radial combining techniques, it is now possible to have solid-state transmitters in *K*-band. The radial combiner, being less lossy as compared to other binary or serial combiners, provides the most economical combining method to achieve the required high output power [3], [4].

This paper describes the results achieved by combining 16 power devices, with Lange [5]–[7] interdigitated couplers and an 8-way radial combiner, to obtain 8.2 W over a 17.7–19.1-GHz frequency band [8]. An advantage of this combining scheme is the graceful degradation of gain and output power in case of one or more device failures.

The system block diagram of the 20-GHz transmitter is shown in Fig. 1. All amplifier modules were designed to have the same mechanical configuration to reduce fabrication costs and allow incorporation of common components wherever possible.

The amplifier uses ten modules which are mechanically identical. The eight combined modules and the second-stage module of the driver are electrically identical. The first-stage module of the driver is identical in electrical topology to the other nine modules; lower power devices have been used, however, for optimum gain performance. A photograph of the completely assembled 8.2-W amplifier with all the associated dc conditioning circuitry is shown in Fig. 2.

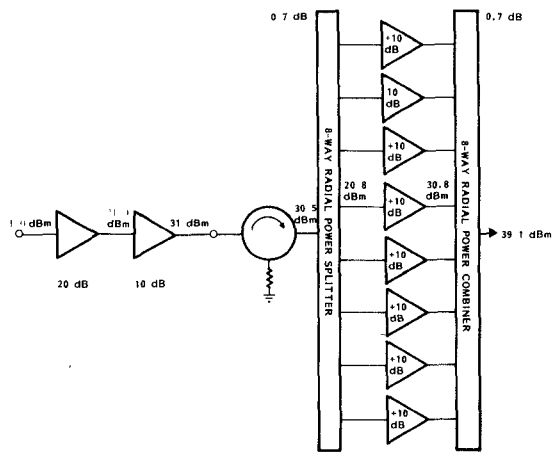

Fig. 1. Block diagram.

II. Device Selection

The device selection is the most important criterion for good amplifier performance. The two important parameters in the device selection are the source inductance and the thermal resistance. Especially in the case of power devices, any additional amount of source inductance can degrade the device gain severely, and thermal resistance is important because of reliability considerations. At this point, there are two possible ways of reducing the source inductance and the thermal resistance simultaneously. One of them is the flip-chip technique, in which the source pads are plated up and the device is mounted upside down on a metallic carrier. This completely eliminates the bond-wire parasitics and provides minimum possible source inductance. At the same time, these plated posts act as a heat sink and are very closely situated to the sources of the heat generated in the active region under the gate. The plated posts in the close vicinity where the heat is generated provide a very low thermal resistance path to the heat sink. This technique is adopted by MSC and Mitsubishi for their high-power devices. The via-hole technique involves etching holes from the reverse side of the device to the source. The device is then gold plated from the reverse side to the

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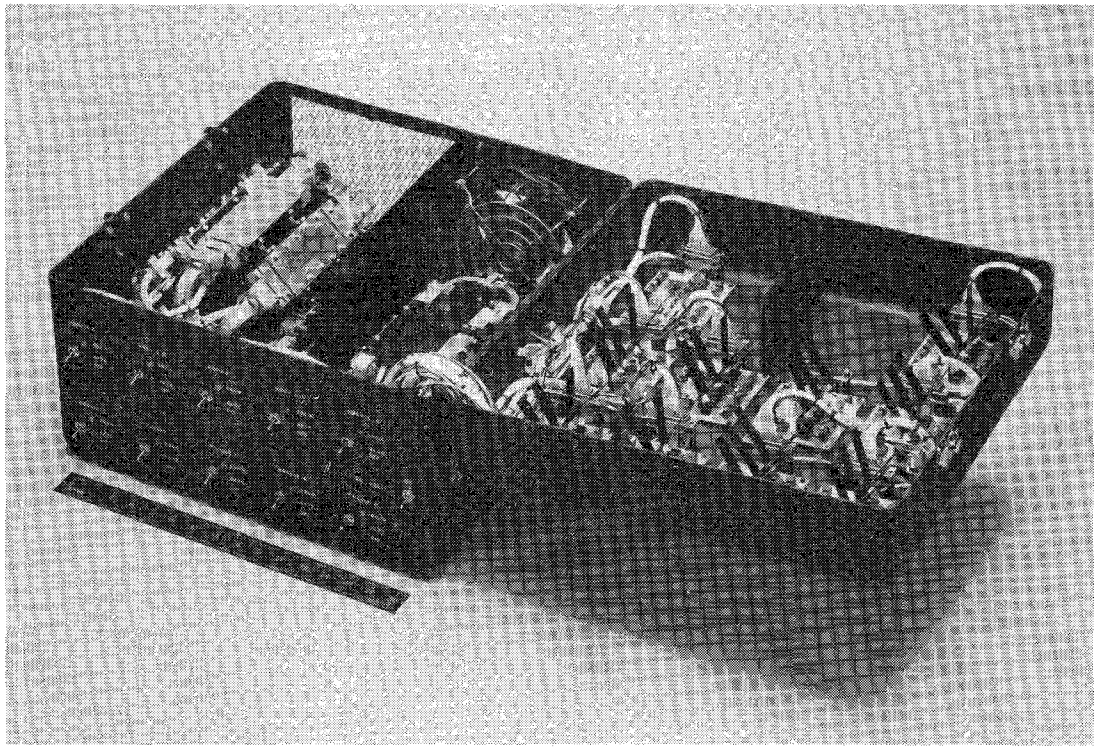

Fig. 2. Complete transmitter amplifier.

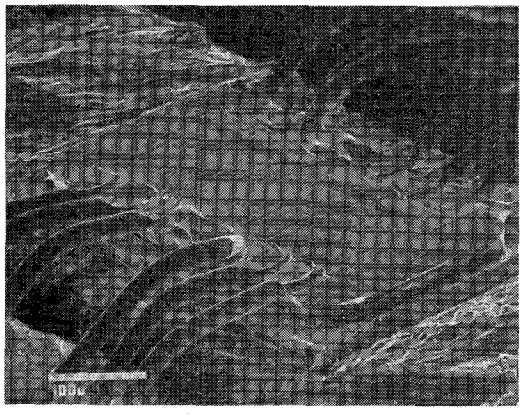

Fig. 3. Raytheon 1.0-W GaAs FET.

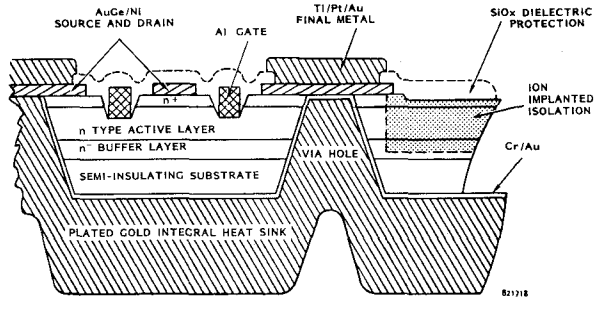

Fig. 4. Schematic cross section through power FET.

source to minimize source inductance and thermal resistance. This technique is used by Raytheon and Bell Labs for their high-power devices up to *K*-band. For this application, Raytheon devices were selected.

Fig. 3 shows the photograph of the typical device used in this amplifier, with Fig. 4 showing the schematic cross section of the power FET with via hole. Devices used in this program have 0.7-μm gate lengths, which are defined by the standard photolithographic process. The wafer flatness and mask bowing limit the gate length to 0.7 to 1.0 μm in the standard photolithographic process. These two factors prevent intimate contact between the mask and wafer over a large area. A 0.5-μm gate definition can be achieved, however, over part of the wafer, but yield is reduced considerably. With state-of-the-art technology, electron-beam lithography can provide 0.4-μm gate lengths. This process also eliminates flatness problems and provides extremely high yields.

III. Amplifier Design

In designing a power amplifier, scattering parameters of the devices are of very little value since they are essentially small-signal parameters and do not provide any information about the input and output impedances required to achieve optimum power. Amplifiers designed by using *S*-parameters yield the maximum gain, but not necessarily the optimum power. To achieve maximum power and efficiency, large-signal characterization of the devices is very important. Large-signal models can be developed by relating transconductance and the output impedance to the operating power levels, but such a method is time consuming.

Electronic load-pull, however, is a faster and more accurate method to determine the desirable load impedance, in addition to measuring the input impedance at rated power. This method of FET characterization is important because

1) it is a real-time measurement; bad data points will be obvious as the measurement is being made;

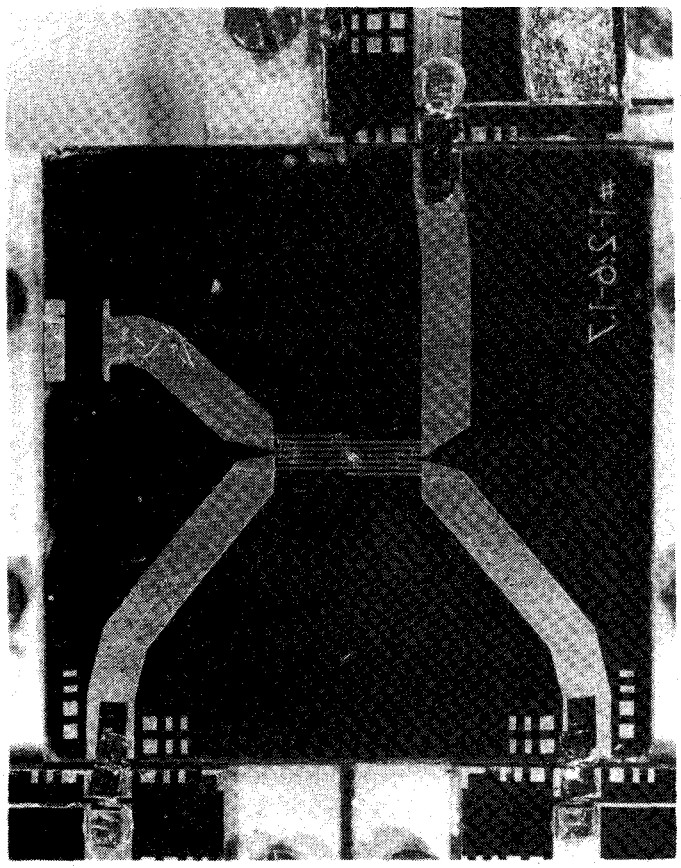

Fig. 5. Six-finger interdigitated coupler.

2) mismatches inherent in tuners, especially at higher frequencies, will not enter in;
3) power out and gain data can be taken simultaneously with impedance data;
4) it allows sorting the devices according to impedances; amplifier designs can thus be more precise and repeatable.

The large-signal parameters were utilized to optimize the input and output matching networks, which offer a conjugate match at the device input and output ports. Computer-aided design was used extensively to optimize the amplifier performance at stage level.

Microstrip was chosen as the transmission medium for fabrication of matching and bias networks. Of the several possible substrate materials, 15-mil quartz was chosen for its advantages of low loss and relatively low dielectric constant. This allows distributed elements to be fabricated in reasonable physical size. An additional advantage of quartz is its rigidity and hardness which allows the use of conventional ribbon and wire bonding techniques for interconnects. Owing to the range of temperatures which may be encountered, thermal matching of the quartz substrate to its supporting carrier was necessary. This was accomplished by utilizing machined carriers of Kovar.

The 3-dB interdigitated couplers were examined for the conventional four-finger configuration. The small gaps required for tight proximity coupling prevented fabrication of traditional four-finger interdigitated couplers on 15-mil quartz substrate, hence, a six-finger coupler was developed for this application. This substantially relaxed the gap and line resolution requirements, making it more reproducible. A 50-Ω termination in the isolated port was realized on the substrate using thin-film techniques. Tantalum nitride Molly-gold metallization was preferred over other metal schemes due to its stability over temperature. The couplers were also mounted on Kovar carriers for the thermal matching considerations. Fig. 5 shows a six-finger Lange coupler fabricated on quartz and mounted on Kovar carriers.

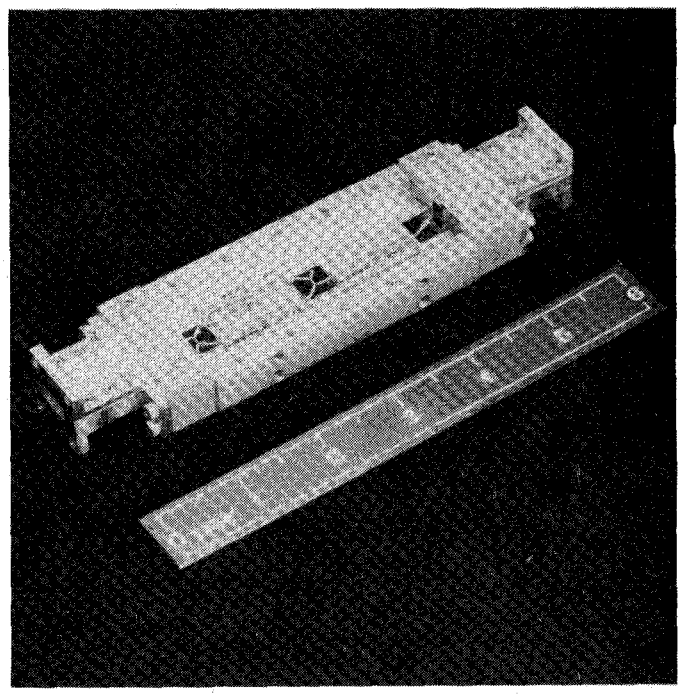

Fig. 6. Driver module.

IV. Module Integration

The module elements are assembled into the final module with the various electrical components pre-tested. These components consist of

1) the input waveguide-to-microstrip transition,
2) the waveguide mode suppressor,
3) the cascaded single-ended amplifier stages,
4) the input Lange coupler for the balanced stages,
5) two cascaded single-ended amplifier stages in balanced configuration,
6) the output Lange coupler for the balanced stages,
7) the waveguide mode suppressor,
8) the output waveguide-to-microstrip transition,
9) the dc feedthroughs to bias the FET's, and
10) other miscellaneous components such as chip capacitors, stand-offs, etc., needed to integrate the module.

All of the components were optimized individually and designed to have sufficient isolation to minimize any effects on performance characteristics due to interaction between the stages. Only minor adjustments were required after integration at the module level.

An assembled driver module is shown in Fig. 6.

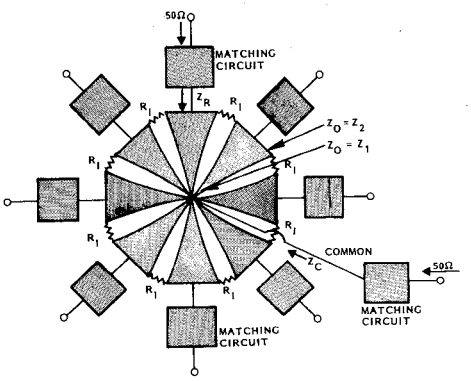

Fig. 7. Radial combiner schematic.

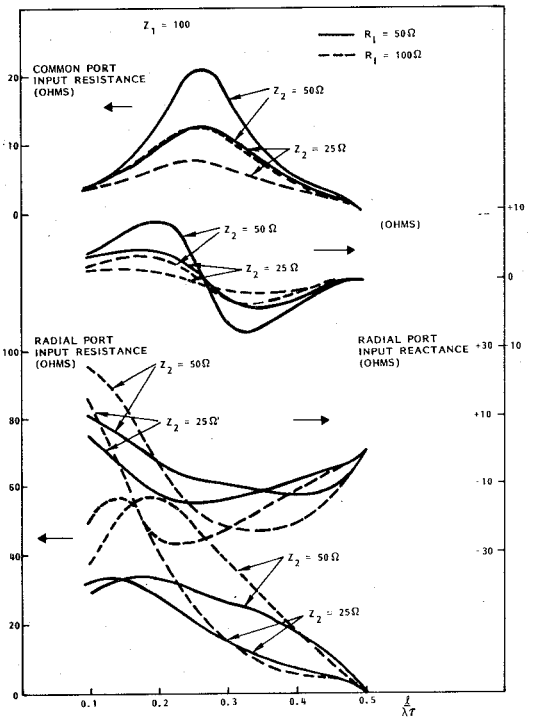

Fig. 8. Combiner computed impedance data.

V. Combiner

The schematic of the combiner is shown in Fig. 7. It comprises eight exponentially tapered transmission lines that connect together at the center to form the common port and are bridged at the radial end by resistors. Identical matching networks on the radial ports match to 50 Ω, and the common port is also matched to 50 Ω.

Fig. 8 shows computed curves of the combiner radial port input impedance $Z_R = (R_R + j \times R)$ and the common port input impedance $Z_C = (R_C + j \times C)$ of the taper fractional wavelength (l/λ_T), taper characteristic impedance (Z_2) at the radial end, and isolating resistor (R_I). The taper characteristic impedance at the common end is set at 100 Ω. The taper wavelength λ_T is related to the uniform line wavelength λ by

$$\lambda_T = \frac{\lambda}{\sqrt{1 - p^2}}$$

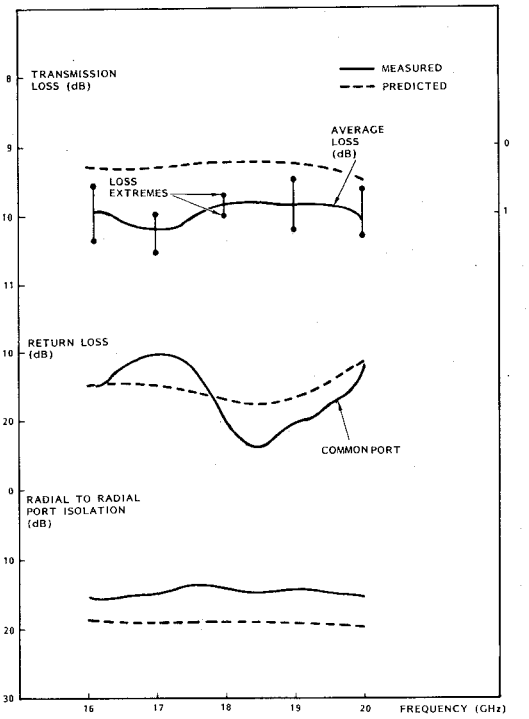

Fig. 9. Combiner measured versus predicted performance.

where p, the taper rate, is given by

$$p = \frac{\log_e(Z_1/Z_2)}{4\pi l/\lambda}.$$

Note that

1) the common port input resistance R_C is largest at a l/λ_T value of approximately 1/4,
2) R_C is largest for a lower value of isolating resistor R_I and higher value of Z_2,
3) radial port resistance (R_R) varies more slowly with frequency for a lower value of R_I, and
4) radial port reactance is lower for a lower value of R_I.

The optimum choice of line length is therefore a quarter-wave, with a high value of Z_2 and low value of R_I.

A computer program was written to model the combiner, in which the matching circuit dimensions, tapered line, and resistor details were allowed to vary numerically. The program calculated the return loss of all ports, transmission loss, and isolation between radial ports. The program took into account, in addition, the coupling between the tapered lines and parasitics of the resistors. The tapered line length was one quarter wave and the resistance value was at 70 Ω. Since the tapered lines must bridge to the resistors, their widths at the low impedance end was set. The even-mode characteristic impedances at the narrow and wide ends of the taper were at 96 and 27 Ω, respectively. Because of the coupling between the tapered lines, their odd-mode impedances were lower than these values.

The common and radial port matching circuits were varied on the computer until a reasonable match was obtained on all ports between 16.0 and 20.0 GHz. No effort was made to adjust the parameters for improvement

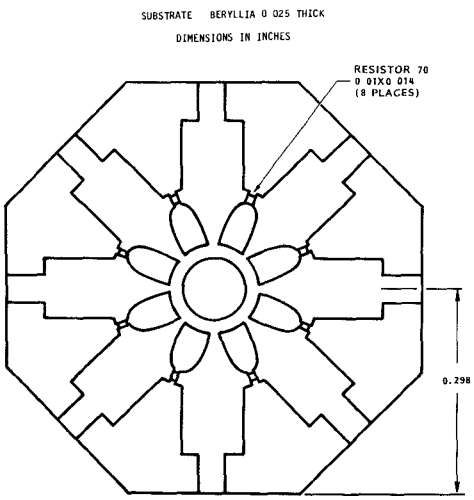

Fig. 10. Combiner microstrip outline.

of radial-to-radial port isolation. The predicted response of the combiner is shown in Fig. 9. The predicted return loss is greater than 11 dB. Radial-to-radial port isolation varies between 15 and 26 dB.

Beryllia was chosen over Alumina mainly due to its lower dielectric constant, which results in higher common and radial port impedances, thus simplifying matching. Also, the thermal conductivity of Beryllia is approximately ten times that of Alumina and, consequently, heat dissipated in the resistors is conducted better to the ground plane. Fig. 10 shows the microstrip outline. The substrate is 0.025-in-thick Beryllia. The radial port matching consists of 29.5-Ω lines of length 0.397 λ at the center frequency. Microstrip lines in 0.43-in-wide troughs connect the radial ports of the combiner to the microstrip-to-waveguide transitions, which are stepped-ridge waveguide types. This design was chosen so that the waveguide resonance of the combiner cavity is above the working frequency.

The measured results of the final combiner are also shown in Fig. 9. The common and radial port return losses are tuned to peak around 18.5 GHz. The maximum VSWR over a 20-percent bandwidth is better than 2:1. The transmission loss is 0.7 dB at band center, of which 0.4 dB can be attributed to the actual combiner substrate dissipation, and the remaining 0.3 dB is due to different transitions. The amplitude unbalance of the eight transmission paths is between 0.25 and 0.8 dB over the range 16–20 GHz. The phase unbalance is $\pm 11°$ at 18 GHz.

VI. Amplifier Integration

All the individual components, i.e., the driver module, the power modules, and the combiner/divider, were fabricated and tested individually. The driver chain, which consists of a cascaded driver module and a power module were tested and exhibited 30.0 ± 0.25-dB gain with 1.25-W output power at the 1-dB gain compression point. The frequency response of the driver chain is shown in Fig. 11.

Eight identical power modules are required in the output stage. In order to achieve the maximum combining efficiency, these amplifiers must be identical not only in

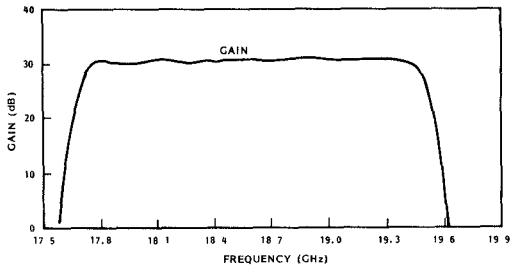

Fig. 11. Frequency response of the driver chain.

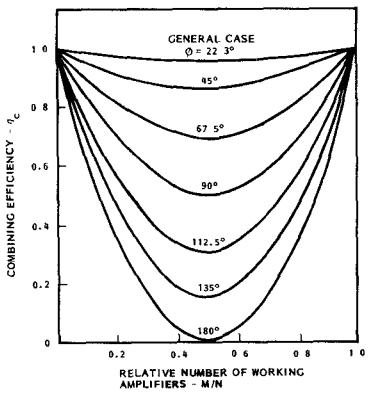

Fig. 12. Combining efficiency degradation as a function of phase variation.

amplitude but also in phase. If the phase of the amplifiers is not identical, then the combiner efficiency is degraded and is given by the following equation:

$$M_c = 1 - 2\frac{M}{n}\left(1 - \frac{M}{N}\right)(1 - \cos\phi)$$

where

M number of amplifiers with identical phase,
N total number of amplifiers, and
ϕ relative phase difference.

Efficiency degradation as a function of phase difference is shown in Fig. 12. It is clear from the graph that in the event two amplifiers are 90° out of phase compared to the other six, then the combining efficiency drops to 60 percent. In order to assure high efficiency, the phase matching of all amplifier modules is required. Each individual amplifier was measured for relative phase. Necessary corrections were made by inserting shims of appropriate thickness in the waveguide interconnect path. Using this technique, all the amplifiers were phase matched within $\pm 2°$ of each other. The output stage was assembled using a divider, eight phase matched amplifiers, and a combiner, as shown in Fig. 13. This output stage was individually checked for frequency response, gain, and output power. Fig. 2 shows the completely integrated amplifier comprised of the driver chain, isolator, output stage, and the associated dc circuitry contained in the cover of the box. Separate switches were provided to turn any individual module on and off to examine the effect of one or more module failures.

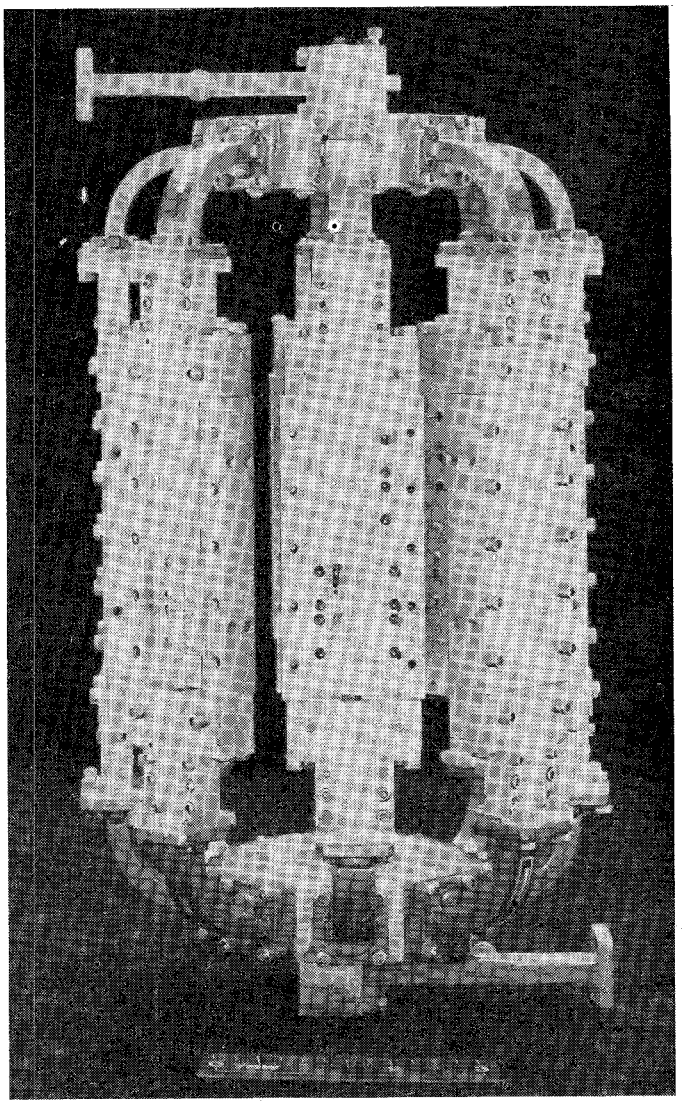

Fig. 13. The output stage.

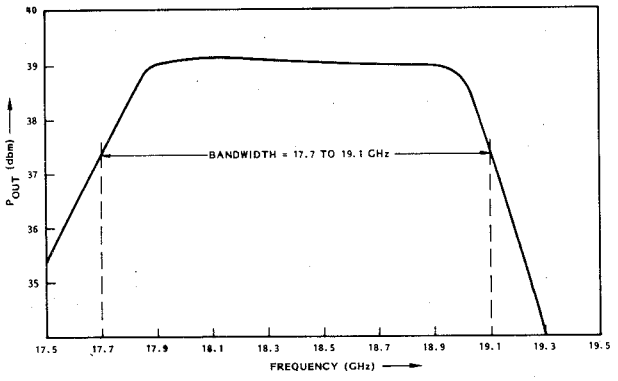

Fig. 14. Transmitter frequency response.

VII. Amplifier Performance

The block diagram of Fig. 1 shows all the gain and power levels at different points. With a 0.7-dB loss in the 8-way divider and combiner and a 0.5-dB loss in the isolator, a 39.1-dBm output power was achieved at the output port. The frequency response of the completed transmitter is shown in Fig. 14. It covers a 17.7–19.1-GHz frequency band with a 39.0-dB gain and ±0.5-dB gain flatness. The transfer characteristic of the transmitter amplifier at 18.4 GHz is shown in Fig. 15. It exhibits 8.2-W (39.13 dBm) output power at 1-dB gain compression point. It also demonstrates excellent power-limiting capability under saturated condition.

The group delay of the amplifier measured from 17.5 to 18.5 GHz is shown in Fig. 16. It exhibits a constant group delay of 8.7 ns with a variation of only ±0.25 ns over a 1.0-GHz band. This is an important parameter in a communication amplifier, which indirectly reflects the excellent

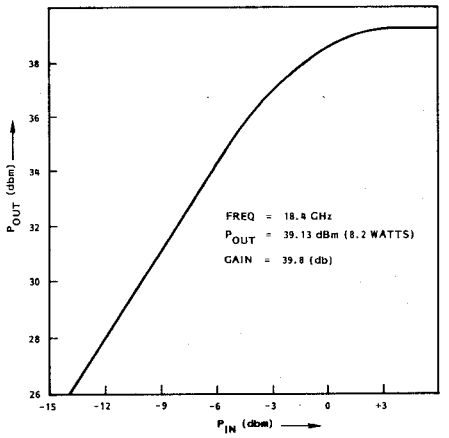

Fig. 15. P_{in}/P_{out} characteristics of transmitter.

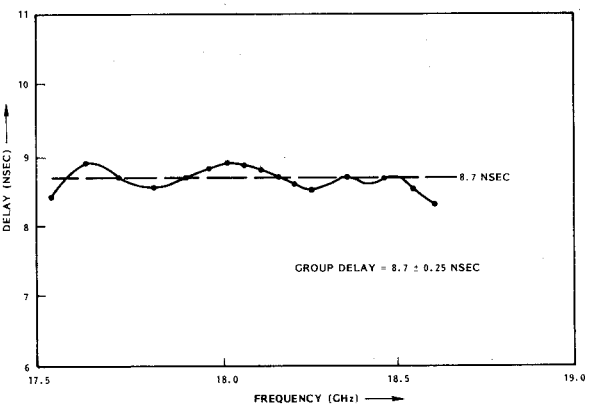

Fig. 16. Transmitter group delay response.

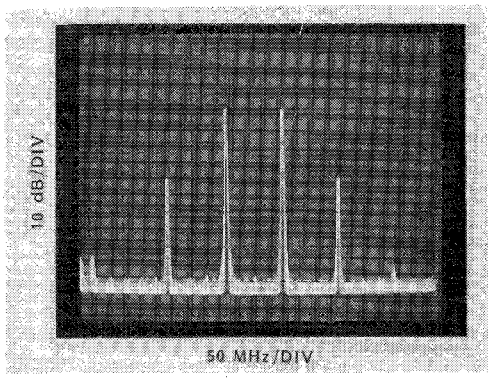

Fig. 17. Transmitter intermodulation characteristics.

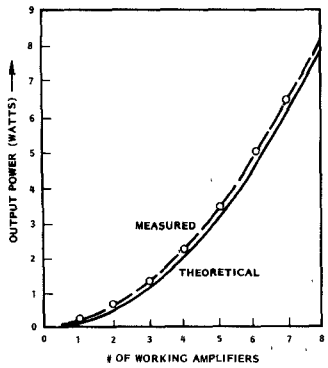

Fig. 18. Theoretical versus measured data on graceful degradation.

phase linearity. AM/PM conversion, another important characteristic of the amplifier, was measured over a 6.0-dB variation in the input power. The worst variation (2°/dB) was observed at the low drive level. The intermodulation performance was measured at different points in the band with two equal amplitude carriers 50-MHz apart. The photograph of Fig. 17 shows the third-order intermodulation distortion at 1-dB gain compression point measured at midband. It was typically 20 dB below either of the two carriers in the complete 1.4-GHz band.

VIII. Graceful Degradation

In the event that one or more amplifiers should fail in the eight-amplifier system shown in Fig. 1, it is highly desirable that the system exhibit the property of graceful degradation. The radial combining scheme provides this feature, meaning that any failed amplifier does not affect the performance of the remaining operating amplifiers, and the greatest possible power is delivered to the output port. The output power of this combiner power amplifier system is related to the number of failed amplifiers by the following relationship:

$$\frac{P_0}{P_m} = \left(\sqrt{k} + -\frac{M}{N}(1-\sqrt{k})^2\right.$$

where

P_0 actual output power,
P_m normal output power with all amplifiers operating,
k the fractional output power of a failing amplifier,
M number of working amplifiers, and
N number of total amplifiers.

This relationship assumes that all the amplifiers are phase matched. This condition was achieved to within $\pm 2°$ in all the amplifier modules used with the combiner.

The total amplifier failure ($K = 0$) was simulated in the output power degradation as a function of the number of amplifier failures was measured and is graphically shown in Fig. 18 by a dotted line. The solid line in Fig. 18 shows the theoretical plot of the above equation. Note that the behavior of the overall amplifier under simulated failures is in close agreement with the classical theory of graceful degradation given by the above equation.

IX. Conclusion

A solid-state power amplifier with 8.2 W over 17.7–19.1 GHz using state-of-the-art GaAs FET devices has been developed. Technologies used for this amplifier, such as the device description, combiner techniques, stage amplifier design, and module integration, are described. Test results of the amplifier indicate a stable design that follows the graceful degradation principle.

Acknowledgment

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Letters

Correction to "Comments on 'The Dynamical Behavior of a Single-Mode Optical Fiber Strain Gage'"

PATRICIO A. A. LAURA AND JOSE L. POMBO

In the first paragraph of Section II of the above paper,[1] the words "Lagrange—Sophie Germaine's" do not belong there.

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Corrections to "New Narrow-Band Dual-Mode Bandstop Waveguide Filters"

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In the above paper,[1] equations (1), (3), (4), and (10) were incorrectly printed due to typographical errors. Following are those equations in their correct form.

$$\begin{bmatrix} e_1 \\ 0 \\ 0 \\ \vdots \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} Z+R & jM_{12} & jM_{13} & \cdots & & jM_{1n} \\ jM_{12} & Z & jM_{23} & \cdots & & jM_{2n} \\ jM_{13} & jM_{23} & Z & \cdots & & jM_{3n} \\ & & & \cdots & & \vdots \\ \vdots & \vdots & \vdots & \cdots & Z & jM_{n-1n} \\ jM_{1n} & jM_{2n} & jM_{3n} & \cdots & jM_{n-1n} & Z+R_n \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ \vdots \\ i_{n-1} \\ i_n \end{bmatrix} \tag{1}$$

$$\begin{bmatrix} e_0 \\ 0 \\ 0 \\ \vdots \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} R_0 & jM'_{01} & 0 & 0 & \cdots & 0 & R_0 \\ jM'_{01} & Z & jM_{12} & jM_{13} & \cdots & jM_{1n} - \dfrac{jM'_{01}}{2m} & 0 \\ 0 & jM_{12} & Z & jM_{23} & \cdots & jM_{2n} & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ 0 & jM_{1n} - \dfrac{jM'_{01}}{2m} & jM_{2n} & jM_{3n} & \cdots & Z & -\dfrac{R_0}{m} \\ m & 0 & 0 & 0 & \cdots & -1 & -m \end{bmatrix} \begin{bmatrix} i'_0 \\ i'_1 \\ i'_2 \\ \vdots \\ i'_n \\ i'_{n+1} \end{bmatrix} \tag{3}$$

$$e'_1 = (Z+R')i'_1 + jM_{12}i'_2 + jM_{13}i'_3 + \cdots + jM_{1n}i'_n$$

$$e'_n = jM_{1n}i'_1 + jM_{2n}i'_2 + \cdots + (Z+R'_n)i'_n \tag{4}$$

$$t' = 1 - \frac{1}{\Delta'}\left(\frac{M'^2_{01}}{2R_0}\Delta'_{11} + \frac{M'^2_{nn+1}}{2R_0}\Delta'_{nn}\right)$$

$$r' = \frac{1}{2R_0\Delta'}\left[M'^2_{01}\Delta'_{11} - M'^2_{nn+1}\Delta'_{nn} + j(-1)^{n+1}2M'_{01}M'_{nn+1}\Delta'_{1n}\right] \tag{10}$$

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[1]J-R. Qian and W-C. Zhuang, *IEEE Trans. Microwave Theory Tech.*, vol. MTT-31, pp. 1045–1050, Dec. 1983.